IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
BAHOUT)
)
Serial No. **Not Yet Assigned**)
)
Filing Date: **Herewith**)
)
For: **METHOD AND DEVICE FOR SEQUENTIAL READOUT OF A MEMORY WITH ADDRESS JUMP**)
)

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

EXPRESS MAIL NO: EL747059966US

DATE OF DEPOSIT: February 22, 2002

NAME: Dawn Kimler

SIGNATURE: Dawn Kimler

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to label FIG. 1 as prior art. FIGS. 1 and 2 are being further modified to label a block therein.

In the Claims:

Please cancel Claims 1 to 6.

Please add new Claims 7 to 29.

7. A method of reading sequentially from a memory having an incremental address counter associated therewith,

the method comprising:

detecting an address jump signal;

incrementing the incremental address counter based upon the detected address jump signal;

reading a content of the memory at the incremented address;

transferring the content read at the incremented address to the incremental address counter; and

reading the content of the memory at the address contained in the incremental address counter.

8. A method according to Claim 7, wherein detecting an address jump signal comprises decoding an instruction code.

9. A method according to Claim 7, wherein the incremental address counter is incremented by at least one unit.

10. A method according to Claim 7, wherein transferring the content read comprises transferring a memory address code corresponding to a following address.

11. A method for reading sequentially from a memory, the method comprising:

providing an instruction code and a memory address code to an input register;

providing the memory address code to an incremental address counter having an input connected to the input register and an output connected to the memory;

reading the memory read at the memory address code indicated by the incremental address counter;

recording contents read from the memory in an output register;

detecting an address jump instruction code using an address jump detection circuit having an input connected to the input register, and an output connected to the incremental address counter;

providing an increment signal from the address jump detection circuit to the incremental address counter based upon the detected address jump instruction code; and

transferring the recorded contents read at the incremented address to the incremental address counter.

12. A method according to Claim 11, wherein the recorded contents comprises a memory address code corresponding to a following address.

13. A method according to Claim 11, wherein the incremental address counter is incremented by at least one unit.

14. A method according to Claim 11, wherein the address jump detection circuit comprises a decoder circuit.

15. A method according to Claim 11, wherein the transferring is performed using a transfer circuit connected to the incremental address counter and to the output register.

16. A method according to Claim 15, wherein the transfer circuit comprises:

a logic gate having an input connected to the output register for transferring in parallel the contents therefrom corresponding to the recorded contents at the incremented address; and

a multiplexer circuit having an input connected to an output of the logic gate, and an output connected to the

incremental address counter for directing thereto either the memory address code in the input register or the memory address code at the incremented address.

17. A device for reading sequentially from a memory, the device comprising:

an input register containing an instruction code and a memory address code;

an incremental address counter having an input connected to said input register for receiving the memory address code therefrom, and an output connected to the memory;

an output register having an input connected to the memory for recording contents read at the memory address code indicated by said incremental address counter;

an address jump detection circuit having an input connected to said input register for detecting an address jump instruction code, and an output connected to said incremental address counter for supplying an increment signal thereto; and

a transfer circuit connected to said incremental address counter and to said output register for transferring the recorded contents read at the incremented address to said incremental address counter.

18. A device according to Claim 17, wherein the recorded contents comprises a memory address code corresponding to a following address.

19. A device according to Claim 17, wherein said address jump detection circuit comprises a decoder circuit.

20. A device according to Claim 17, wherein said transfer circuit comprises:

a logic gate having an input connected to said

output register for transferring in parallel the contents therefrom corresponding to the recorded contents at the incremented address; and

a multiplexer circuit having an input connected to an output of said logic gate, and an output connected to said incremental address counter for directing thereto either the memory address code in said input register or the recorded contents at the incremented address.

21. A device for reading sequentially from a memory, the device comprising:

an input register containing an instruction code and a memory address code;

an incremental address counter having an input connected to said input register for receiving the memory address code therefrom, and an output connected to the memory;

an output register having an input connected to the memory for recording contents read at the memory address code indicated by said incremental address counter;

an address jump detection circuit having an input connected to said input register for detecting an address jump instruction code, and an output connected to said incremental address counter for supplying an increment signal thereto;

a logic gate having an input connected to said output register for transferring the contents therefrom corresponding to the recorded contents at the incremented address; and

a multiplexer circuit having an input connected to an output of said logic gate, and an output connected to said incremental address counter for directing thereto either the memory address code in said input register or the recorded contents at the incremented address.

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22. A device according to Claim 21, wherein the recorded contents comprises a memory address code corresponding to a following address.

23. A device according to Claim 21, wherein said address jump detection circuit comprises a decoder circuit.

24. A device according to Claim 21, wherein said logic gate transfers the contents from the memory to said multiplexer circuit in parallel.

25. A device comprising:

a microprocessor;

an input register connected to said microprocessor for receiving an instruction code and a memory address code therefrom;

an incremental address counter having an input connected to said input register for receiving the memory address code therefrom;

a memory having an input connected to an output of said incremental address counter;

an output register having an input connected to said memory for recording contents read at the memory address code indicated by said incremental address counter;

an address jump detection circuit having an input connected to said input register for detecting an address jump instruction code, and an output connected to said incremental address counter for supplying an increment signal thereto; and

a transfer circuit connected to said incremental address counter and to said output register for transferring the recorded contents read at the incremented address to said incremental address counter.

26. A device according to Claim 25, wherein the recorded contents read at the memory address code indicated by said incremental address counter are read sequentially from said memory.

27. A device according to Claim 25, wherein the recorded contents comprises a memory address code corresponding to a following address.

28. A device according to Claim 25, wherein said address jump detection circuit comprises a decoder circuit.

29. A device according to Claim 25, wherein said transfer circuit comprises:

a logic gate having an input connected to said output register for transferring in parallel the contents therefrom corresponding to the recorded contents at the incremented address; and

a multiplexer circuit having an input connected to an output of said logic gate, and an output connected to said incremental address counter for directing thereto either the memory address code in said input register or the recorded contents at the incremented address.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after

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the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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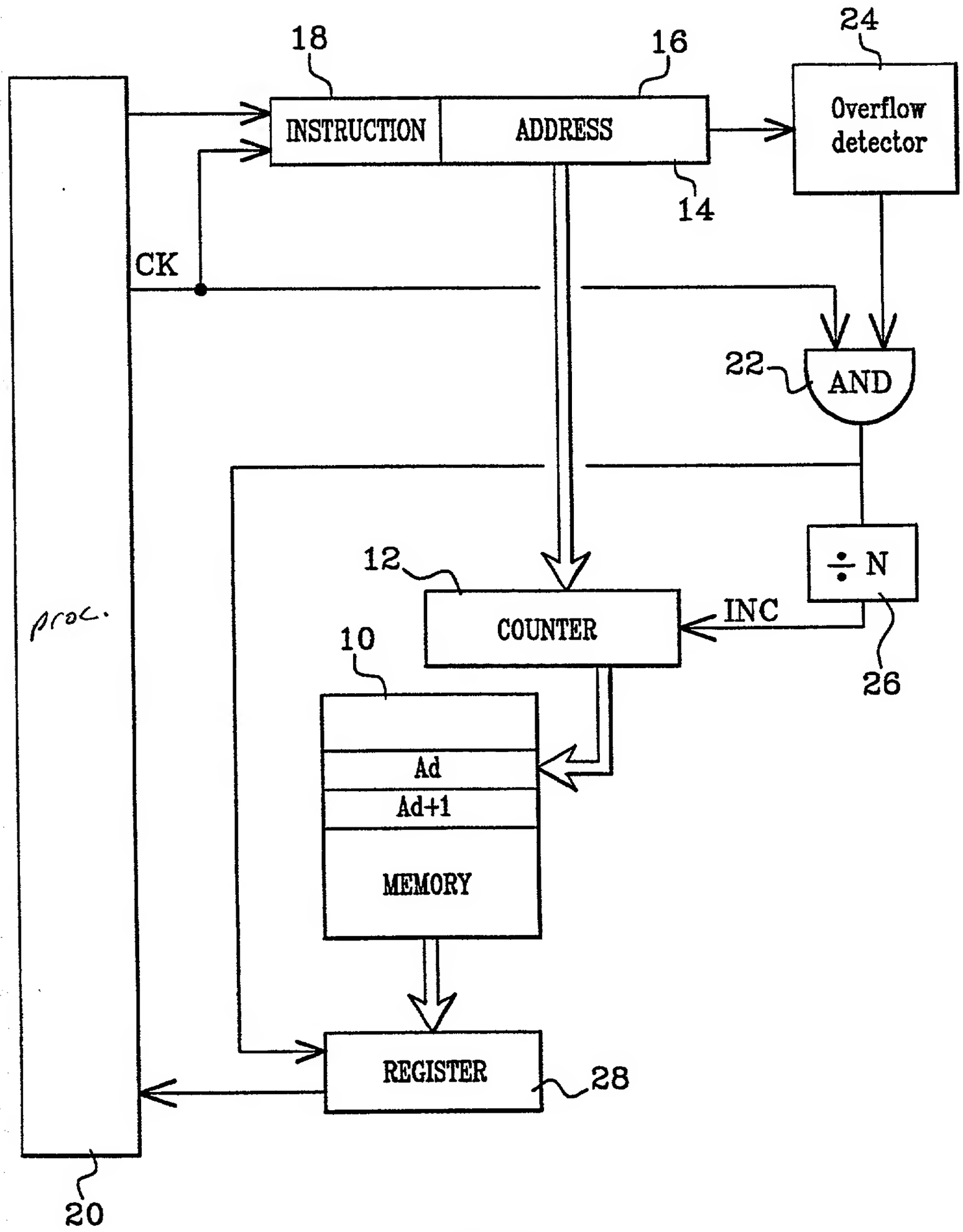

Fig. 1

(Prior Art)

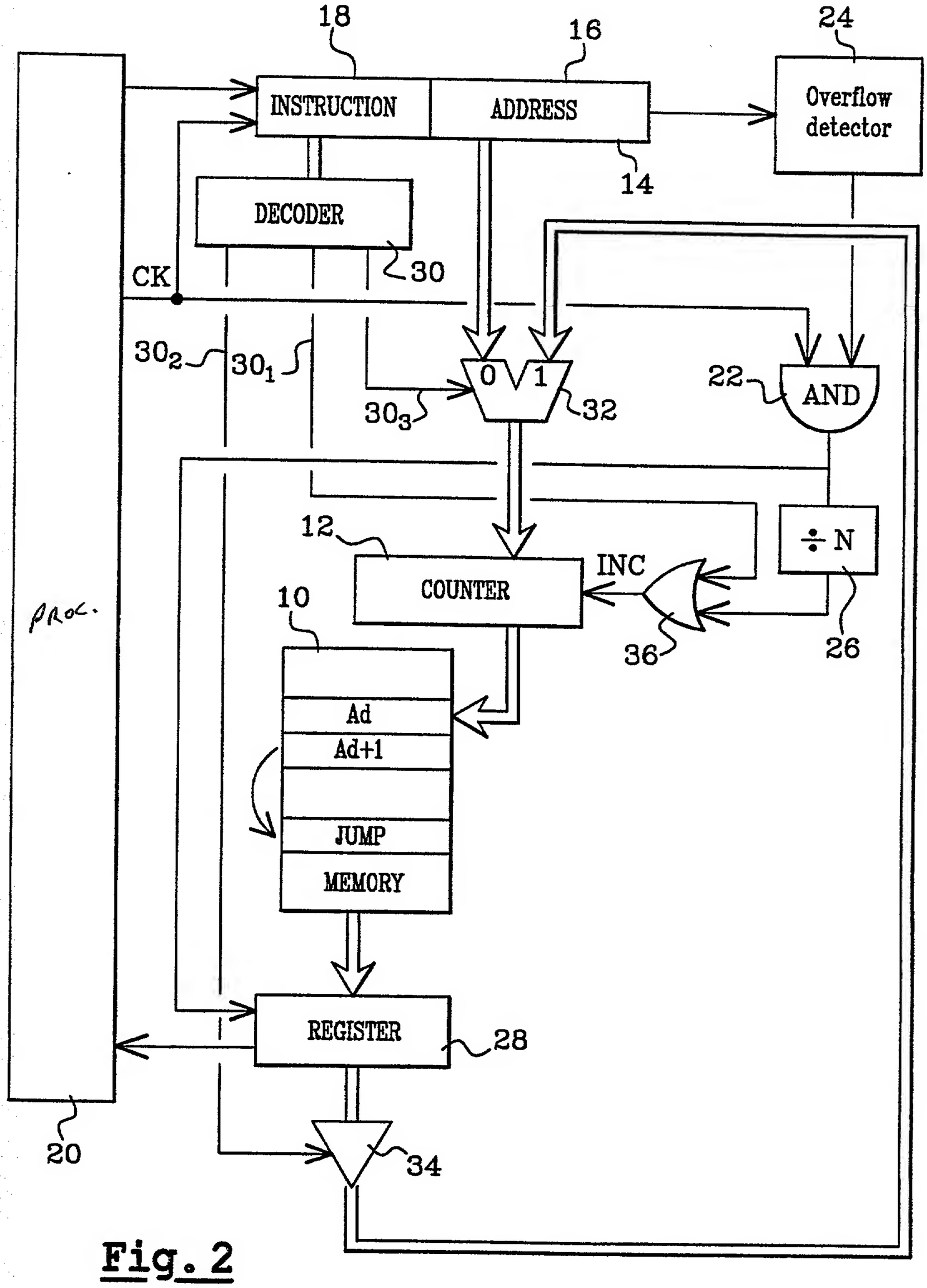
18
16
24
INSTRUCTION
ADDRESS
Overflow detector
14
DECODER
CK
30
30_2
30_1
30_3
0
1
32
22
AND
12
COUNTER
INC
÷N
10
36
26
Ad
Ad+1
JUMP
MEMORY
REGISTER
28
20
34

Fig. 2